AMENDMENTS TO THE SPECIFICATION

Please amend the specification at page 19, beginning at line 1 as follows:

Fig. 1 schematically shows an entire structure of a semiconductor integrated circuit according to a first embodiment of the present invention. Referring to Fig. 1, a semiconductor integrated circuit 1 includes a memory internal circuit 2 to carry out data input/output in synchronization with a clock signal CLK, a boundary scan test circuit 3 to test the electrical connection of a pin terminal of a semiconductor integrated circuit 1, a control circuit 4 for setting boundary scan circuit ~~30~~ 3 to an operable/disabled state, and a power on detect circuit 5 detecting application of power supply voltage VDD to output a power on detect signal POR.

Please amend the specification at page 19, beginning at line 10 as follows:

Boundary scan test circuit 3 executes a test operation according to an input signal JTG applied to a pad 6a when ~~operates~~ operational. Control circuit 4 selectively sets boundary scan test circuit 3 to an operable state or disabled state according to the potential of pad 6b. Pads 6a-6c are bonding option pads. A bonding wire is selectively connected according to the sealing package type or an internal operation function mode. Here, a bonding option pad includes both a pad that has bonding between a pad and a pin terminal selectively made, and a pad that has wiring to a corresponding pin terminal selectively made. A bonding option pad has a programmable potential.